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Materials Technology for Environmentally Green Micro-electronic Packaging

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ABSTRACT

Intel has been continuously striving to provide environmentally green micro-electronic packaging solutions for high-density interconnect (HDI) product applications. The environmentally green initiative consisted of providing lead-free (Pb-free) packaging materials solutions as well the enabling of halogen-free (HF) substrates technology to eliminate the use of brominated flame retardants. This paper discusses the challenges overcome by Intel to deliver on both aspects of environmentally green packaging. Although Intel's efforts to enable Pb-free and HF-compliant packaging solutions have been wide-ranging, the scope of this paper is limited to discussing the key technology development challenges faced in transitioning to Pb-free materials in first-level interconnects (FLI), second-level interconnects (2LI), solder thermal interface materials (STIM) applications, and halogen-free (HF) substrate materials. The transition to Pb-free micro-electronic packaging materials and HF substrate technology required a paradigm shift in the industry, needing extensive benchmarking initiatives and sharing cross-technology learnings across the industry and academia. The delivery of Pb-free packaging solutions across FLI, 2LI, and STIM applications as well as HF substrate technology has strongly reinforced Intel's One Generation Ahead (OGA) philosophy in micro-electronic packaging.

INTRODUCTION

Intel's drive to "get the lead out of the package" began over five years ago when we produced a Pb-free tin-silver-copper (SAC) solder for 2LI applications that complied with European Union Restriction of Hazardous Substances (EU RoHS) requirements. Continuing on this path to deliver "Pb-free" packaging, Intel recently reached a critical milestone by eliminating Lead (Pb) from the FLI solders in its next-generation 45nm Silicon technology roadmap products. Intel is among the first semiconductor companies to deliver Pb-free FLI solutions in high-volume manufacturing. In order to meet the stringent integration challenges of transitioning to Pb-free-compliant packages, Intel has also successfully developed substrate, FLI flux, and underfill (UF) materials technologies that are compliant with higher Pb-free processing temperatures. Intel has been working with suppliers, customers, and several industry consortia to develop and provide EU RoHS-compliant products. Intel has completed certification of EU RoHS-compliant materials and processes and is manufacturing and shipping many EU RoHS-compliant products today. Additionally, in anticipation of the RoHS regulations, Intel pro-actively worked to develop pioneering Pb-free STIM materials to

meet the challenging needs of heat dissipation from the silicon die.

Intel's drive to enable halogen-free (HF) substrate technology entailed a careful evaluation of HF material properties to identify robust materials sets in order to meet manufacturing, assembly, performance, and use condition-based reliability criteria. The selected HF substrate materials sets were fungible with existing manufacturing and assembly processes used previously with nHF (not halogen-free) cores. Several technical challenges were overcome in enabling the HF substrate technology. Mechanical drilling of HF cores, as well as substrate warpage, was evaluated to verify that their performance was on a par with nHF cores, from a manufacturing and assembly perspective. The electrical properties of the HF core material were also evaluated and it was determined that the impact on performance compared to that of nHF cores was negligible. From a reliability perspective, the key concern with HF substrates was delamination, which can occur due to moisture release at Pb-free reflow temperatures from the HF core material. To verify that adequate reflow delamination margins exist for HF substrates, relative to use condition requirements, a component reflow accelerated test was developed by Intel and used to assess Intel's HF product lineup. The drive to enable HF materials has continued with the development and successful introduction of HF-compliant packaging materials such as molding compounds, underfill materials, and Polymer TIMs.

In the first half of this paper, we discuss Intel's qualification of Pb-free packaging solutions in the first-level interconnect (FLI), second-level interconnect (2LI) and solder thermal interface materials (STIM) applications. In the second half, we address the enabling of halogen-free (HF) substrates and accompanying reliability challenges.

A schematic of a lidded ball grid array (BGA) Intel package is shown in Figure 1 which depicts the FLI, 2LI, TIM, and substrate materials technologies that are undergoing the environmentally green transition in Intel's micro-electronic packaging.

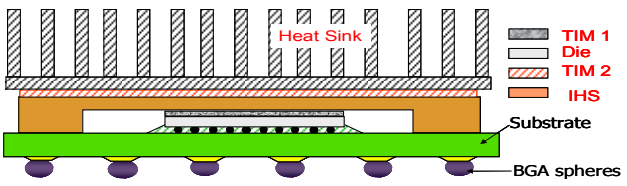


Figure 1: Schematic of Intel's lidded BGA package

PB-FREE INITIATIVE: FIRST LEVEL INTERCONNECT MATERIALS (FLI)

Intel recently announced the achievement of a significant milestone in the quest to deliver RoHS-compliant Pb-free FLI solutions in micro-electronic packaging. The transition to Pb-free FLI interconnects that connect the silicon die to the substrate eliminated the last 5% of Pb remaining in the package. Traditionally, tin-lead solder alloy has been used for FLI chip-to-substrate and 2LI substrate-to-board attachment interconnect materials. The presence of lead in tin-based solder alloys, mostly with the composition of eutectic 63Sn-37Pb, lends the solder superior thermal and mechanical characteristics for microelectronic assembly and reliability. However, the inherent toxicity of lead has raised serious environmental and public health concerns. Developing lead-free alternative solder alloys for micro-electronic substrates is of paramount importance. Intel selected tin-silver-copper (SAC) solder metallurgy as the lead-free chip attachment material for its 45nm CPU products. Compared to their tin-lead counterpart, high tin content, lead-free C4 solders possess physical properties less desirable for assembly and reliability: higher surface tension, increased mechanical stiffness, and a higher melting point. A number of technical challenges have been encountered and solved during Intel's lead-free C4 interconnect development. For example, reduced wettability of lead-free solder with die copper bumps can pose challenges to the downstream underfill process. Moreover, optimization of substrate solder metallurgy has also shown to be very effective in improving the mechanical robustness of the C4 interconnect, and in minimizing the occurrence of C4 brittle solder joints. The change to Pb-free SAC solder alloy necessitated the development of alternate flux materials to clean off the more tenacious tin oxides from the solder surface and form a robust FLI solder joint. The new flux material needed to be stable at high process temperatures as well as be cleanable following the chip attach process to allow strong adhesion between the underfill, the bump metallurgy, and the die passivation. The formation of a robust FLI, Pb-free joint significantly increased the current carrying capability of the joints. The transition to Pb-free FLI solder materials also necessitated the development of underfill materials technology designed to mitigate additional thermo-mechanical stresses imposed on the die due to stiffer FLI joints.

Changing from a Pb-based C4 substrate solder to a Pb-free metallurgy drove an increase in the peak reflow temperature during die attach in assembly requiring Pb-free-reflow-compliant substrate materials technology. The selection of the dielectric materials set (core material, buildup layer, and solder resist) in the Pb-free substrate was therefore critical to ensure robust reliability

performance of the package at higher reflow temperatures. In particular, the glass transition temperature (Tg) and the coefficient of thermal expansion (CTE) values of the dielectric materials set were carefully selected to minimize the risk of substrate warpage, substrate dielectric material cracking, and die damage.

Thus, along with changing the solder alloy material to one that is Pb-free, a judicious choice of the associated materials sets allowed Intel to solve the challenge of removing the remaining 5% of lead, thereby achieving EU RoHS-compliant FLI packaging technology.

PB-FREE INITIATIVE: SECOND LEVEL INTERCONNECT MATERIALS (2LI)

Another critical challenge to meet EU RoHS requirements in Intel's packaging technology was the transition to Pb-free solder technology for 2LI applications. 2LI refers to the interconnect between the substrate and the printed wiring board (PWB). 2LI is accomplished with solder sphere, flux and/or paste, and it involves two reflow processes: ball attachment (BA) and surface-mount reflows for board attach. In the BA process, paste is printed onto the metal pad on the BGA side of the substrate, typically by using screen printing. Then solder spheres are picked and placed onto the paste printed pads. Finally, substrates with solder balls undergo a reflow process, typically in a multizone convective oven. In the surface process, solder paste is applied onto the metal pad on the PWB, typically by using stencil printing. Solder ball-attached packages are then picked and placed onto the fluxed PWB. Finally, the entire package and PWB undergo a reflow process typically in a multizone convective oven. Traditionally, eutectic tin-lead alloy was used for 2LI solder metallurgy applications. Relatively low melting temperatures (T_m = 183°C) and excellent shock resistance of the eutectic Sn-Pb alloy made this alloy highly suitable for Pb-ed BGA applications. Several Pb-free solder alloys for BGA applications were evaluated for this purpose, and SAC405 (tin-4% Ag- 0.5% Cu) was downselected based upon extensive materials characterization and reliability evaluations. The SAC405 solder alloy has a higher melting temperature (217-221°C) than eutectic SnPb solders, as well as a higher elastic stiffness and yield strength. These differences in the physical and mechanical properties of SAC405 solder alloy posed several challenges to packaging processes and reliability performance, especially due to the need to reflow the solder alloys at much higher temperatures (230-260°C peak reflow temperatures) than those used for eutectic SnPb. Figure 2 shows a typical SAC solder alloy reflow profile (BA and SMT) used for SnAgCu solder.

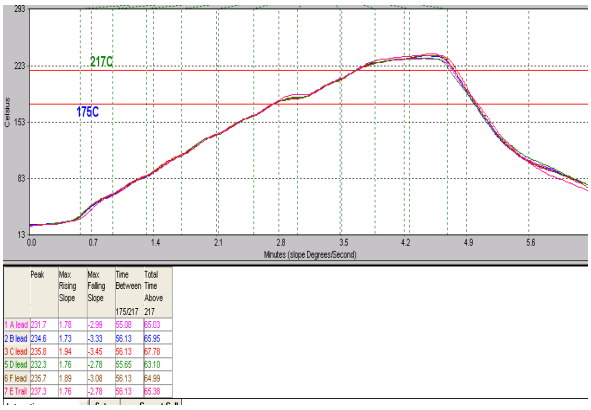


Figure 2: Typical SAC solder alloy reflow profile (BA and BGA)

The transition to Pb-free solders also necessitated a change in the composition of the paste from eutectic SnPb to SAC405 metal powder paste for BA and surface-mount applications. This change in paste composition forced the need to optimize the fluxability of the flux in the paste to ensure robust solder joint formation in conjunction with the SAC405 solder BGA spheres. Higher processing temperatures necessitated the use of appropriate solder paste/flux formulations that could withstand the higher thermal exposure and facilitate excellent joint formation with a myriad of surface finishes such as Electroless Nickel Immersion Gold (ENIG), Cu OSP (Organic Surface Protection), and Immersion Silver (ImAg). The use of SAC solder alloy for BGA applications has the potential to impact both the package- and board-level manufacturing and reliability. Additionally, Intel's packages also utilize paste for attaching BGA spheres to the packages. As mentioned earlier, the need to reflow SAC solders at higher temperatures impacts the package and board materials manufacturing to enable high temperature reflow. In addition to the metallurgical challenges involved in the high temperature reflow of 2LI solder joints, the impact of high temperature reflow on the viscoelastic behavior of the package and board-level materials and accompanying reliability concerns needed to be understood. In the next section, we discuss the 2LI solder joint reliability challenges and board-level surface-mount challenges due to the transition to Pb-free materials.

Pb-free Initiative: 2LI Reliability Challenges

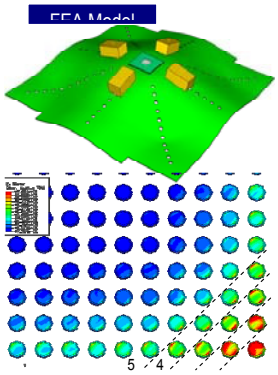
A failure-mechanism-based approach was used for Lead-free (LF) 2LI reliability assessment. An LF material property comparison was made with SnPb solder to understand the failure-mechanism-based reliability risks. The typical LF reliability concerns based on the failure

mechanism and stress testing approach are listed in Table 1.

Table 1: LF failure concerns and recommended stress testing

LF Failures Concern	Stress Test	Comments
Solder fatigue	Temp Cycle	Electrical open/solder crack
Overstressing	Shock Test	Electrical open/solder crack
Overstressing	Vib Test	Electrical open/solder crack
PCB trace, via corrosion	Temp/Humid 85/85°C	Electrical open due to via, trace corrosion
IMC growth, Diffusion and Solder creep	Bake Test	Electrical open IMC growth, diffusion, & shorts due to solder creep

LF 2LI reliability challenges include delamination with increased reflow temperature (35° C higher than Sn/Pb), lower mechanical margin in high strain rate shock testing due to increased stiffness (1.5 times stiffer than SnPb solder), creep performance difference compared to SnPb, and Sn whiskers. The JEDEC specification for max reflow spec of 260° C was established as part of the solution, and Intel components were qualified to meet the JEDEC specification for peak reflow requirements. Use-condition-based reliability performance was used for Pb-free alloy selection. The LF mechanical margin was lower than that for SnPb solder, but it passed intensive board-level shock and vibe testing. The mechanical margin testing showed lower mechanical performance compared to SnPb solder, and the results are shown in Figure 3. The NCTF design rule was implemented at corner joints for shock margins.



Solder	Crack (%)Row				
	Non CTF		CTF		
	1	2	3	4	5
Sn/Pb	50	0	0	0	0
LF	100	20	0	0	0
Sn/Pb	50	50	0	0	0
LF	100	100	40	0	0
Sn/Pb	100	75	0	0	0
LF	100	100	100	100	100

Figure 3: Mechanical margin assessment for LF solder

The failure mode during shock is manifested in cracking along the solder joint (either on the package or board side) as shown in Figure 4 [1].

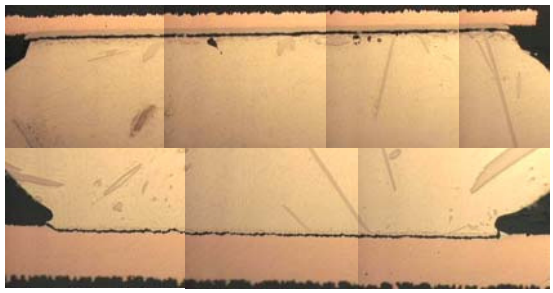


Figure 4: SAC405 solder joint failure in shock conditions

A detailed failure analysis reveals that the shock crack in SAC is along the interface between the IMC and the solder (package side) and through the IMC bulk (board side). In either case, shock failure is characterized by a lack of solder deformation and an absence of solder bulk cracking. This is quite contrary to thermal fatigue failure where the solder joint exhibits extensive inelastic deformation that is often time-dependent.

This difference is partly due to the strain-rate sensitivity of metallic materials. Metallic materials including solders typically become stronger with increasing strain rates. In other words, the flow stress increases with increasing strain rates. The strain rate sensitivity is a strong function of the homologous temperature (T_{hom}), which is considerably higher for solders, due to their low melting temperatures.

As a result of the high strain rate sensitivity, the yield strength of SAC solders increases rapidly with strain rate. This increased yield strength suppresses any plastic deformation and prevents the shock energy from dissipating through the solder joint, thereby transferring more stress to the interface which causes interfacial fails. The yield strength of eutectic SnPb solder is relatively low compared to the SAC405 solder alloy. This means SnPb solders can dissipate more high strain rate energy through deformation and hence can perform better in shock than a SAC405 solder alloy. The higher yield strength of the SAC405 solder alloy is derived primarily from the precipitation hardening of the tin matrix by the Ag_3Sn precipitates/platelets. In addition to the increased bulk strength of the SAC alloy, the higher reflow temperatures can also cause an increased thickness in the IMC layers and thereby degrade the shock performance of the SAC405 solder alloy. However, the increased strength of the SAC405 solder alloy is beneficial for thermal cycle fatigue resistance as it reduces creep damage in each

thermal cycle. Thus the transition from eutectic SnPb to SAC405 solder alloy poses more challenges in high strain rate shock applications, but provides more margin in thermal cycle reliability.

The LF fatigue performance was about 20-30% higher than SnPb for Flip Chip Ball Grid Array 9FCBGA (FCBGAs). Temperature cycle results are compared with the SnPb solder as shown in Figure 5. LF (SAC405) showed improved fatigue performance in both 15-min. and 30-min. dwell time testing.

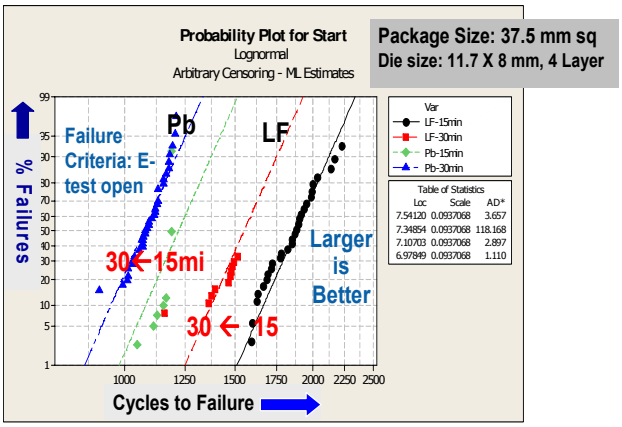


Figure 5: LF temp cycle performance comparison with Sn/Pb solder

LF creep performance concerns were addressed through long dwell time testing. Long dwell time temperature cycle testing (three cycles/day) were completed for SAC405, and the results showed better LF performance than SnPb solder as shown in Figure 6 [2].

Figure 6: LF Temp cycle performance in long dwell time testing

The industry concern over long dwell time was satisfactorily addressed based on these results, and the LF reliability model correlation showed a similar type of fit compared to that of Sn/Pb solder. The corrosion and diffusion concerns were addressed through temperature humidity testing (85/85 test) and bake test (125°C) for 1000 hrs. Bake testing did not show interface-related failure mechanisms. The results are shown in Figure 7.

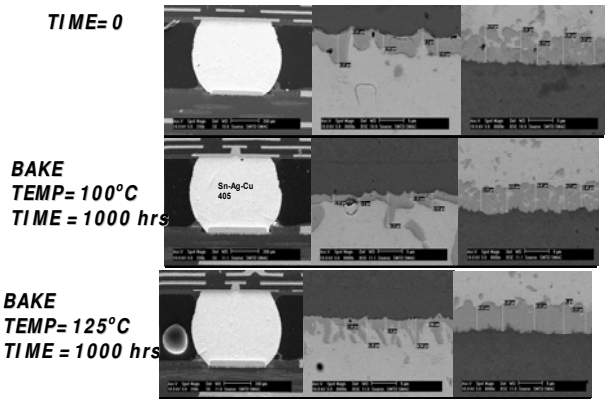


Figure 7: Bake test results for SAC405 with Im/Ag SF

The other LF reliability concern is the formation of tin (Sn) whiskers. Sn whisker formation is not an issue for Pb-free solders, but concerns the Sn surface finish on components. The Sn whisker failure mechanism is an electrical short caused due to the growth of the whisker. An example of Sn whiskers is shown in Figure 8 [3].

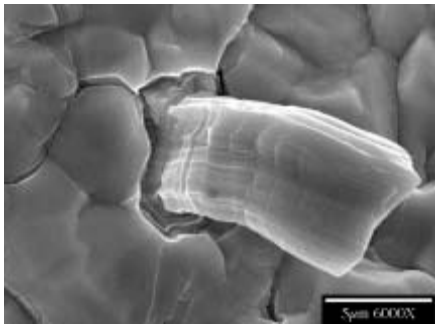


Figure 8: Sn whiskers

The concern about Sn whiskers for Sn-coated components is not related to LF issues, but it is the same as that for Sn/Pb solder. JSTD 201 was established for Sn whisker mitigation that includes the use of matte Sn and anneal at higher temperatures for stress relief prior to SMT.

PCB surface finish quality characteristics have an impact on reliability: micro void associated with Im/Ag PCB SF quality characteristics negatively impacted the solder fatigue margin (40-50% reduction in temperature cycle performance). The impact of micro void on temperature cycle performance is shown in Figure 9. The other concern is a Kirkendall-type void in bake testing for OSP

SF. Kirkendall-type voids were attributed to Cu purity and OSP chemistry and are related to the coating process. Proper control of PCB plating quality mitigated the micro void risk for Im/Ag and Kirkendall-type void for OSP SF.

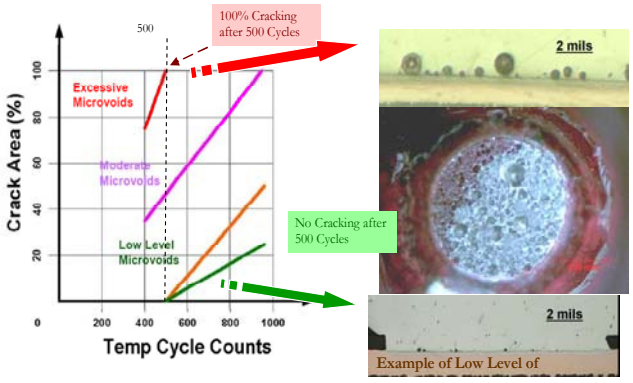


Figure 9: Impact of micro void on temperature cycle performance

Pb-free Initiative: Surface-Mount Challenges

The transition to Pb-free solders for 2LI posed severe challenges to surface-mount technology, and an equivalent effort in adapting board manufacturing and SMT processes was required. The transition affected not just the SMT pastes used in board assembly, but also wave solders and board materials. Process steps significantly affected by the conversion are shown shaded in pink, with their impact described in Figure 10.

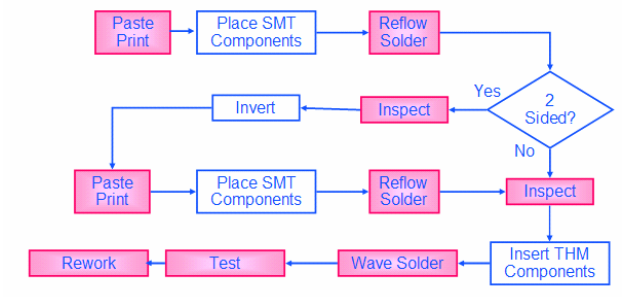


Figure 10: SMT process flow diagram indicating impact due to Pb-free transition

Solder Paste Printing

The same stencil printing equipment, stencil fabrication technology, and stencil thickness used for SnPb can be used for Pb-free solder pastes. If reduced stencil aperture openings (when compared to the land area) are being used for SnPb pastes, these apertures will need to be expanded to cover the entire land area, since Pb-free solders do not wet out to the same extent as Pb-ed. The most popular Pb-free solder paste composition is SAC305.

Component Placement

Component placement is only marginally affected by the change to Pb-free solder. SAC solders are more grainy and less shiny than SnPb solders. There can also be a wider part-to-part variation in solder appearance. When front-side lighting is used for component lead or ball recognition, such as for BGAs, these differences may require adjustments to the vision system hardware and/or algorithms, to properly recognize Pb-free solder balls and surfaces.

Reflow Soldering

Since SAC305 has a higher initial melting point (217°C) than Sn-Pb (183°C), higher reflow soldering temperatures are required as shown in Figure 11. Wetting characteristics of SAC305 are not as superior as that of SnPb. This requires a slightly longer reflow soldering window, typically 230 to 250°C for Peak Reflow Temperature with 40 to 120 seconds above 217°C. Since this window is narrower than that used for eutectic SnPb, a greater level of control is required for Pb-free reflow soldering, and this necessitates better reflow soldering ovens. Ten zone ovens are typical for Pb-free reflow, instead of the seven zone ones sufficient for SnPb. Higher temperatures also lead to deleterious effects on the boards. Metallic surfaces not covered with solder paste during reflow soldering will get more oxidized than for SnPb, degrading the wetting of these surfaces during subsequent soldering processes, such as wave soldering. Using a nitrogen atmosphere in the reflow oven will mitigate this oxidation to a large extent. Higher reflow temperatures also increase PCB warpage, increase risk of delamination and blistering, and weaken the plated through-hole (PTH) copper. PCB laminates with higher glass transition temperatures, higher thermal degradation temperatures, longer time to delamination at temperatures at and above 260°C, as well as lower z axis expansion coefficients, will all help alleviate these issues.

Wave Soldering

SAC305 and eutectic SnCu are two alloys used for Pb-free wave soldering. Both have higher melting points (217°C and 227°C, respectively) than SnPb. Thus, an increased solder pot temperature is required, in the 260-275°C range, rather than the 250-260°C range. Increased temperatures may require a different wave solder flux, one that reaches an optimum activity level at a higher temperature. A new wave solder pot and machine are required to avoid cross-contamination between Pb-free and SnPb solders.

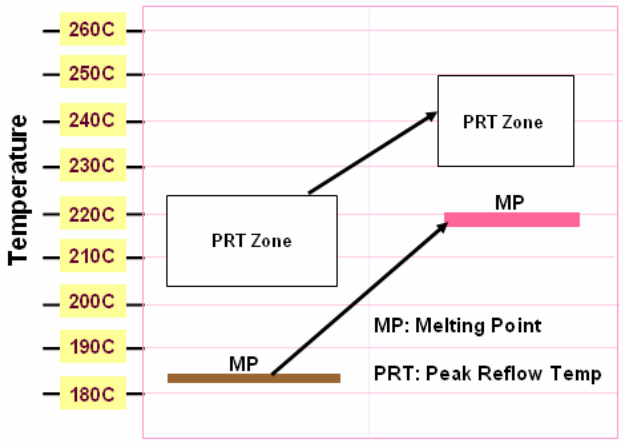


Figure 11: Comparison of peak reflow temperature ranges between eutectic SnPb (L) and SAC (R) alloys

Since the Pb-free solders have diminished wettability under the same flux activity levels, filling PTHs to achieve strong reliable through-hole solder joints and adequate coverage of test point pads becomes a challenge, especially when using surface finishes such as OSP, which is prone to oxidation at higher temperatures. Examples of acceptable and unacceptable wave solder filling are shown in Figure 12. Some ways to mitigate these challenges are increasing flux application density, achieving adequate penetration of the flux in the through holes, and using a turbulent chip wave option. The latter, however, increases the dissolution and erosion of the copper lands and traces, and it also increases copper content in the solder pot. Since the melting points of Pb-free alloys increase quite markedly with an increase in the copper content, an effect that also reduces the fluidity of the solder wave, the copper content needs constant monitoring to avoid certain defects.

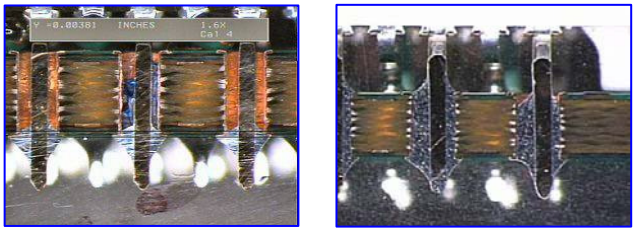


Figure 12: Unacceptable wave solder hole fill (L) and acceptable hole fill (R)

In-Circuit Test (ICT)

Higher reflow and wave soldering temperatures cause two issues for In-Circuit Test (ICT). One, board test points collect extensive polymerized flux residue. This results in a larger build-up of this flux residue on test probe tips and barrels. Consequently, the test probes have to be cleaned more frequently in order to control retest rate increases caused by probe contamination. Two, there is increased oxidation of test points on the board. This results in higher contact resistance, which increases false failures, raising the retest rate and reducing the capacity of the test area. Probes with higher forces, sharper points, or rotating action can reduce the contact resistance issues with Pb-free boards, but can also cause board damage due to board flex and damage at test points. Using a nitrogen atmosphere during reflow and/or wave soldering can significantly reduce surface oxidation of the test points, but this will increase process costs. Also, because Pb-free solders are harder than SnPb, probe tips wear out faster, requiring more frequent replacement.

Solder Joint Inspection

SAC solder joints are typically less shiny and more grainy than eutectic SnPb joints as shown in Figure 13. SAC solder joints also spread less on lands and pads than SnPb joints. For these reasons, both manual and automated visual inspection criteria need to be adjusted for Pb-free board assemblies. Due to the lack of Pb, a heavy element, SAC solder has lower stopping power for x-rays. This causes x-ray images to appear a lighter shade of gray in transmission X-ray images used for inspection of solder joints that are not visible, such as BGA and QFN joints. Hence, Automated X-ray Inspection (AXI) criteria may also require adjustment.

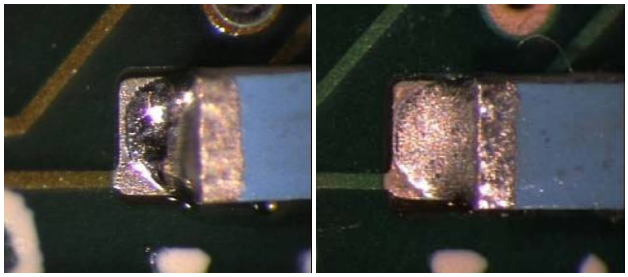


Figure 13: Visual inspection difference between SnPb solder joint (L) and SAC solder joint (R)

Rework

Repair and Rework become increasingly more difficult for Pb-free board assemblies, mainly due to the higher temperatures required for removing and replacing defective components. A greater amount of rework temperature control is required for Pb-free assemblies and this increases the total rework time in most cases. Due to the different solders, soldering irons and other equipment need to be changed from those used for SnPb rework. The risk of damage to the PCB lands, pads, and laminate is also increased, especially when there is direct contact between hotter soldering irons and the pads, such as during the Site Redressing process step for BGA component rework. Thinning of the copper thickness in the PTH barrel is significantly increased during the mini-pot rework process for connectors and other through-hole

components as shown in Figure 14. The higher tin content of the SAC solders causes more copper dissolution and erosion, increasing barrel thinning. Use of newer Pb-free alloys can alleviate this copper dissolution/erosion to a large extent.

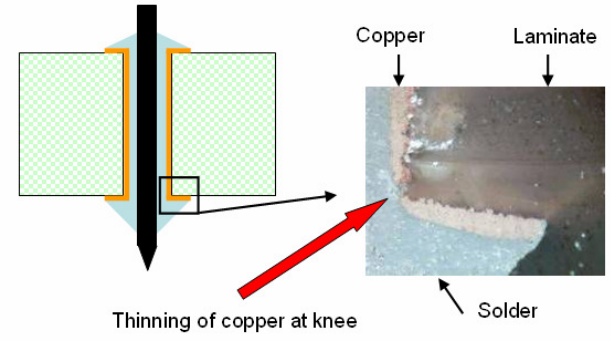


Figure 14: Copper erosion from minipot rework

Pb-free Initiative: Customer Manufacturing Enabling Challenges

Given the significant challenges posed in the SMT materials and processes to enable Pb-free transition, an equivalent effort was needed to influence and enable the ODM and OEM customer base to adopt the Pb-free technologies and processes. The efforts undertaken by Intel to influence the industry are outlined in this section. Customer enabling for Pb-free board assembly consisted of multiple steps over four years prior to the July 2006 RoHS date.

1. A customer-ready document, informally called the Pb-free Manufacturing Advantage Service (MAS), was prepared to capture technical learnings from the Intel Lead Free Board Assembly Team (LFBAT). It included tutorial information on all Pb-free board assembly modules in a typical production line, and also the Intel Reference Process for each module, with detailed process parameters and process material selections. It served as a starting point for customer process development. The Pb-free MAS, containing a substantial wealth of information, was developed in order to meet customer's requirements for more detailed information.
2. Customer Manufacturing Enabling (CME), a new group at the time, engaged major ODM and OEM customers, delivered the Pb-free MAS in person (primarily in APAC), and invited certain customers to participate in further enabling activities.
3. One challenge with developing a board-level process was the limited availability of Pb-free boards and components. The CME team developed Pb-free test boards, with Pb-free Bills of Material (BOMs), representing designs from desktop, mobile, and server market segments. Selected customers in each segment were provided with board designs, or physical boards, and BOMs, or physical parts, depending on their preference.
4. Customers used the board kits (typically 75 boards) to develop a board assembly process on their own. Both Intel and customers then performed reliability tests on samples of the boards and shared results.
5. After results from the development builds were incorporated into customer processes, customers completed another round of builds with Intel representatives present, using additional Pb-free board kits. These were called validation builds, intended to confirm that the customer process could consistently produce good boards over a larger quantity (up to 200) in a manufacturing environment (rather than a lab), without tweaking the process mid-build. Again, Intel and customers separately performed reliability testing, Failure Analysis (FA), and Materials Analysis (MA) and again, shared results.
6. Intel and customers held Manufacturing Readiness Assessment meetings to review all results and customer status regarding their own further development work and builds of prototypes.
7. After the launch of Pb-free products, Intel monitored customer manufacturing performance during launch and ramp, providing assistance as needed.

By this process, Intel ensured a smooth launch and ramp for the initial Pb-free platforms in each segment. In addition, it helped drive industry convergence on a narrow set of Pb-free materials that allowed Intel to produce Pb-free components with only one ball alloy for all desktop, mobile, and server products.

PB-FREE INITIATIVE: SOLDER THERMAL INTERFACE MATERIALS (STIM)

Intel's foray into Pb-free materials in electronic packaging began more than five years ago through the introduction of STIM in the 90nm technology node products. The relentless progress of Moore's law, leading to a doubling of transistor density in silicon chips every generation, drove the need to develop thermal solutions to dissipate additional heat generated in the silicon die. Consequently, Intel's packages have evolved from a bare die solution catering to mobile market segments to Integrated Heat Spreader (IHS) lidded products in desktop and server market segments as shown in Figure 15 [4].

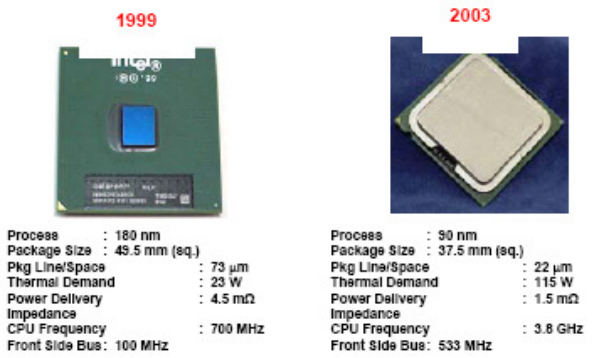


Figure 15: Evolution of Intel's Package technology for meeting thermal performance requirements

There are several technical and cost drivers to enable lidded thermal architecture such as minimizing the impact of local hot spots by improving heat spreading, increasing the power-dissipation capability of the thermal solutions, expanding the thermal envelopes of systems, developing thermal solutions that meet business-related cost constraints, as well as developing solutions that fit within form-factor considerations of the chassis.

The primary role of the IHS is to spread the heat out evenly from the die and to provide a better bondline control of the interface material. This can be achieved by increasing the area of the IHS and by using a high thermal conductivity thermal interface material with low interfacial resistances. In order to meet thermal dissipation targets, Intel introduced polymer thermal interface materials (PTIM) initially with 3-4 W/m^{o}K bulk thermal conductivity and then successfully transitioned to Pb-free solder-based thermal interface material to meet the ever increasing demand for thermal cooling capability as shown in Figure 16 [5].

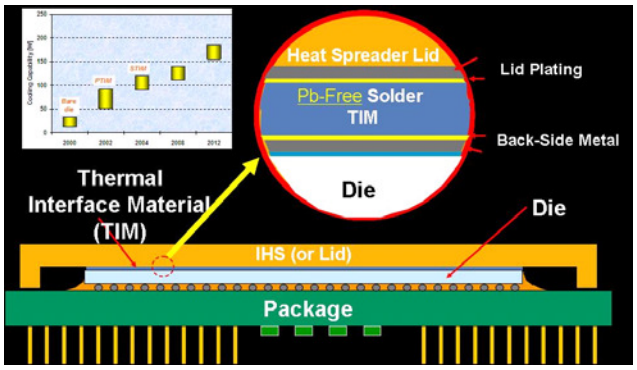


Figure 16: Improvement in thermal cooling capability with TIM materials (Polymer vs. Solder)

The introduction of Pb-free solder-based TIM materials posed significant integration challenges. The STIM needed to relieve the mechanical stress caused by CTE mismatch of the integrated heat spreader lid and the silicon die and to minimize stress transfer to the silicon die during thermal cycling [6]. The thermal conductivity and the mechanical compliance requirements resulted in the development and qualification of low melting temperatures (157^{o}C T_m), low mechanical yield strength (4-6 MPa), and relatively high thermal conductivity (~87 W/m^{o}K) pure Indium (In) metal for STIM applications. In order to use In for STIM applications, appropriate flux vehicles had to be developed to a) effectively reduce the thermodynamically stable native Indium oxide on In performs; b) to control solder joint voiding post joint formation; c) to control interfacial reactions with surface finishes on the IHS lid and the back side metallization (BSM) on the silicon die; and d) to deal with reliability issues faced in small and large die products, such as thermal fatigue cracking of the Indium during thermal cycling. The assembly process, including the reflow of the Indium STIM to form uniform intermetallic compounds (IMCs) post assembly, is a key challenge. A schematic of the STIM microstructural development as a function of packaging assembly steps is shown in Figure 17. The Indium oxide on the surface of the Indium needs to be effectively reduced in order to form uniform and defect-free intermetallic layers at both the die/Indium and the IHS lid plating (Ni/Au) and the In. Indium oxide is an extremely tenacious and thermodynamically stable oxide as shown in Figure 18 [7]. The presence of voiding in the joint can potentially lead to an increase in local thermal resistance and consequently lead to the degradation of the thermal performance of the joint. Additionally, excessive spallation of the binary Au-In IMCs as well as the formation of excessive Kirkendall voiding due to relatively different diffusion coefficients of In-Au and Ni can result in an increase in the thermal resistance of the joint.

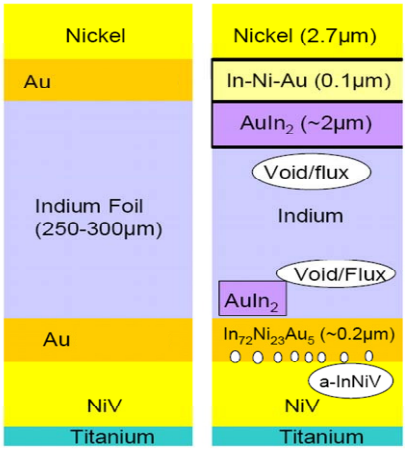


Figure 17: Use of Indium metal as STIM and interactions with surface finish on IHS and BSM pre and post assembly

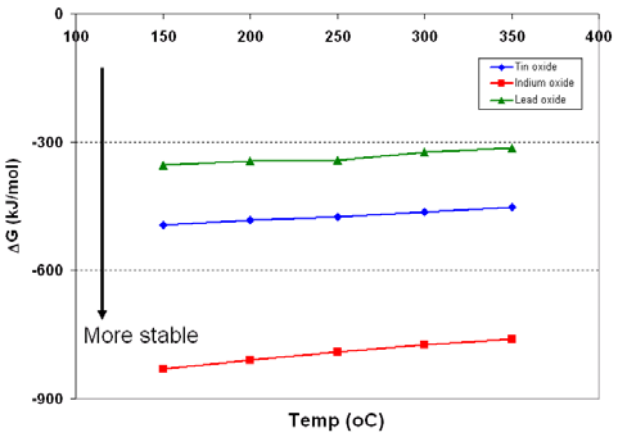


Figure 18: Thermodynamic stability of Indium Oxide as a function of temperature

In reliability testing as in thermal cycling, tensile and shear stresses are imposed on the STIM joint due to the mechanical coupling of the die to the IHS lid and the package as shown in Figure 19.

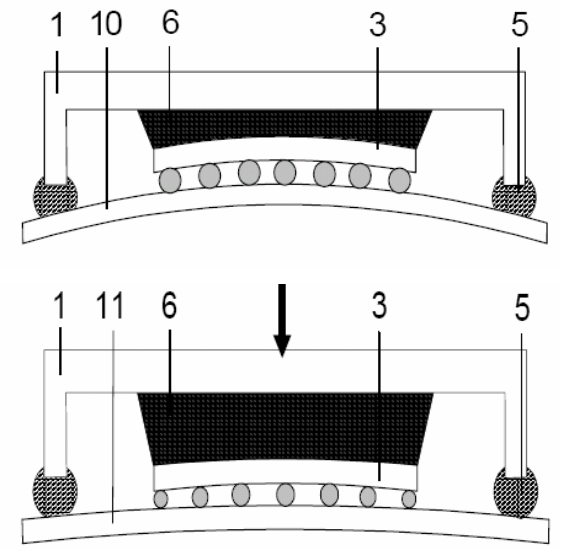


Figure 19: Warpage induced stresses on STIM joint at low temperature and high temp thermal cycling (Numbers in figure indicate different locations along package)

Typical failure modes encountered in STIM joints relate to thermal fatigue cracking of Indium close to the IHS/Indium interface which is manifested in the form of a white signature in CSAM imaging as shown in Figure 20 [6].

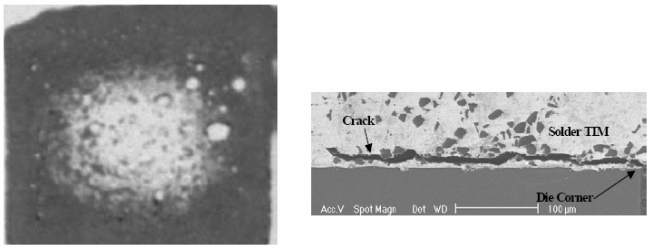


Figure 20: White CSAM image showing delamination at the Indium/IHS interface and corresponding cross-section SEM image showing cracking post reliability testing

The reliability performance of the STIM joints has been found to be modulated by the relative thickness and morphology of the binary and ternary IMCs as influenced by the fluxing ability of the flux used and the reflow profile used, as well as several mechanical design attributes of the IHS dimensions/die size, package stiffness, and preform dimensions. In addition to the technical challenges faced in enabling Indium, a significant effort was made to establish a strong supply chain for IHS lid manufacturing and plating, sealant materials technology for attaching the IHS lid to the substrate, as well as the development of appropriate back side metallization on the die to enable interfacial reactions with STIM to ensure robust joint formation.

In summary, Intel's transition to Pb-free packaging materials technology was attained through a judicious choice of materials across all functional areas such as FLI, 2LI, and STIM. The Pb-free materials solutions met all the integration assembly and surface-mount challenges as well as component and board-level reliability requirements. Intel worked closely with industry partners including suppliers and the ODM and OEM customer base to achieve a smooth launch and ramp of the Pb-free packaging materials technologies.

We now discuss Intel's stewardship in enabling HF-compliant packaging materials initiatives specifically the enabling of HF substrates technology.

HALOGEN-FREE PACKAGING MATERIALS INITIATIVE

As part of Intel's broad strategy to support an environmentally sustainable future, Intel is introducing environmentally conscious HF and Pb-free packaging at the 45nm CPU and 65nm chipset technology nodes. HF packaging materials introduced by Intel include several materials such as molding compounds, underfill materials, and substrates. The scope of this section of this paper is limited to HF-compliant substrate technology. Historically, components and printed circuit boards

(PCBs) have used nHF flame retardants, which have been the subject of an environmental impact debate for a number of years. Primary concerns regarding nHF flame retardants include bioaccumulation and toxic dioxin formation during recycling. Intel's drive to meet HF requirements in substrates is to substantially reduce the Br and Cl levels in the substrates to meet HF requirements, which are currently being established by industry consensus.

Table 2: Comparative core material properties

Core	Tg (°C) TMA	CTE (ppm/C)			Modulus (GPa)		Peel Strength (kN/m)	Dielectric Constant	Dissipation Factor	Moisture Absorption (%)
		x1,x2	y1,y2	z1,z2	25°C	260°C		@ 1 GHz	@ 1 GHz	
Halogenated	176	12,11	11,10	22,166	21	11	1.1	4.6	0.009	0.07
HF	172	13,10	12,11	15,130	23	10	1.0	4.7	0.018	0.05

A key component in Intel's HDI package that requires conversion to HF is the substrate, which is the focus of HF enabling in this paper. Typically, nHF substrates contain Br and Cl-based compounds in the core material, the buildup dielectric layers, the solder resist, and the PTH plug material. To enable HF substrates, each of the above mentioned materials was changed over time. A schematic cross-section of a package is shown in Figure 21.

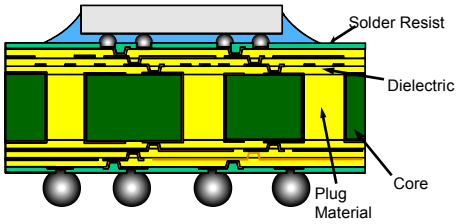


Figure 21: Assembled substrate schematic, labeled with key material items that required a change to HF

Intel has several years of HVM experience with HF dielectric, plug and solder resist materials, and hence the final push to enable HF substrates required a change to the core material, wherein the HF core does not contain brominated flame retardants. HF core material candidates, which meet Intel's assembly and reliability criteria, have been identified, and these are presented in the next sections.

HF Core Material Selection

Challenges

The ideal HF core material is one that can serve as a "drop-in" solution, with material and reliability properties that meet or exceed those for nHF core material. By close matching of material thermo-mechanical and electrical properties, the degree of change to substrate manufacturing, assembly, board-level reliability, and performance can be minimized. Table 2 shows a sample comparison of nHF vs. HF core material properties, where x1, x2 refers to CTE in the x direction below Tg (x1) and above Tg (x2). As indicated in Table 2, the thermo-mechanical and electrical properties of selected nHF and HF cores were similar. This enabled a relatively smooth conversion from the standpoint of assembly, 2LI reliability, and electrical performance.

The mechanism for flame retardency in nHF vs. HF core materials is different, due to differences in the flame retardant used in the core. nHF cores typically use a brominated flame retardant, wherein the Br reacts with combustion reactant species, suppressing reaction propagation and creating a layer of char, both of which help to stop the fire. In contrast, HF core materials typically use a metal hydrate as the flame retardant, wherein the metal hydrate releases water to cool the polymer and simultaneously creates a char passivation layer:

Metal hydrate + heat → char + water

In practice, use of HF core materials in Pb-free packages can be challenging, because the HF core tends to undergo more decomposition/water release at Pb-free reflow temperatures (~260°C). This is due to differences in the flame retardant type and content in HF vs. nHF cores. This poses a challenge specifically for BGA component reliability, as a significant amount of moisture release from the core during repeated Pb-free reflows (for BA, board mount, etc.) can facilitate delamination in the substrate as shown in Figure 22.

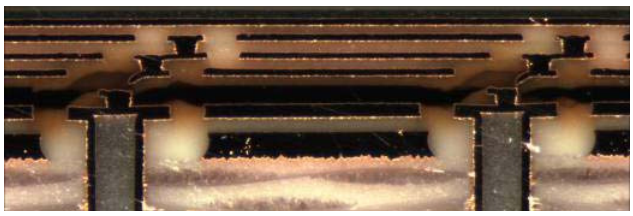


Figure 22: Cross-section of HF substrate, which has suffered a delamination in the buildup layers

To address this concern, a reflow accelerated test best known method (BKM) was implemented and used in the HF core material downselection process. The reflow accelerated test BKM incorporated JEDEC Pb-free Level 3 preconditioning (L3 precon) [8] with stepwise, additional Pb-free reflows (@ 260°C), to check for the delamination margin in the HF product substrates. Up to 15x additional reflows (beyond L3 precon) were run to test the delamination margin. Through careful material selection and screening, robust core materials, that met Intel's reliability requirements, were identified.

HF Core Material Results

HF core material selection required us to focus on substrate manufacturing, component and board-mount assembly, reliability testing, and performance. The results from these evaluations are presented in the following sections.

Substrate Manufacturing

From the substrate manufacturing perspective, the key challenges were selection of robust core materials, followed by mechanical drilling and flatness assessments of those materials. To select the most robust core materials, substrate suppliers were engaged and enabled with the reflow accelerated test BKM. Thorough evaluations were performed on various short and full loop test vehicles (TVs) with different designs, to understand the impact of core material and design on delamination reliability. Based on the number of reflows before the occurrence of delamination, the core materials with the most robust heat resistance were selected for further evaluation. These core materials were confirmed to be HF at Intel through ion chromatography testing, with the Br and Cl contents measuring <4 ppm. Core material drillability, as well as drill bit life parity between nHF and HF core, was established across the substrate supply base through drilling evaluations on the downselected materials. The parity in drill bit life ensures that there is no increase in drilling costs when an HF core is used. By measuring substrate flatness on incoming substrates, it was shown that HF core and nHF core units were equivalent across the substrate supply base.

Intel Assembly

The above trend carried forth through Intel assembly, wherein HF substrate flatness was the key assembly concern. Figure 23 shows comparative HF vs. nHF BGA ball coplanarity data for a 13x14mm TV. The data confirm that HF and nHF cores have similar flatness performance.

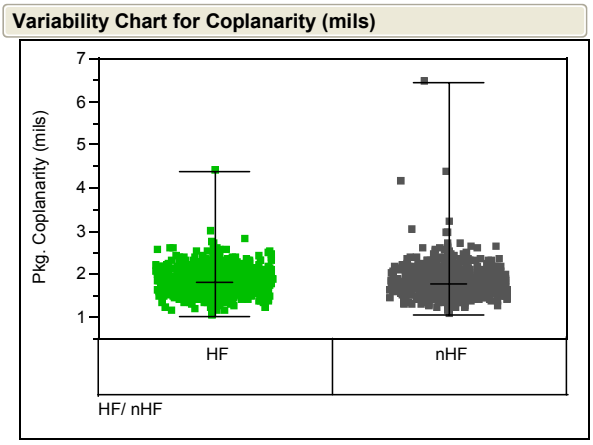


Figure 23: Comparison of HF to nHF package coplanarity for 13x14 mm TV

Board mount of nHF vs. HF components was also studied, with results indicating similar board-mount yields for both nHF and HF units.

HF Substrates Component Reliability

Reliability testing at the component level involved use of Intel's new Pb-free L3 preconditioning plus up to 15x additional reflows at 260°C, to check for delamination margins. A number of HF core materials were dropped from consideration because of delamination margins. The selected HF core materials were robust during reliability testing, and for the given form factors/designs in Table 3, passed more than 10x additional reflows beyond L3 preconditioning before any delamination was observed. Reliability results were similar for substrates across Intel's supply base, indicating sufficient reliability transparency.

HF Substrates Enabled Reliability

Enabled reliability testing (component mounted on the board) also showed performance parity between nHF and HF core TVs as shown in Table 4. In shock testing (a.k.a. dynamic bend testing), neither nHF nor HF substrates showed cracks in any critical to function (CTF) BGA solder joints.

Flammability Rating

Due to concern about flame retardant decomposition during multiple Pb-free reflows for BGA products, and the potential implications of this for flammability rating, a check of the UL-94 flammability rating before and after extended Pb-free reflows was done. Table 5 shows the results, which indicate that both nHF and HF core materials were able to maintain a V-0 flammability rating after 10x Pb-free reflows.

Table 3: Example HF core component reliability performance for different form factors

Substrate Form Factor	Reliability Stress	HF Core Related Fails
13x14 mm	L3 Precon + TCB (-55°C / +125°C)	0/149 post 750 cycles
	L3 Precon + HAST (130°C/85% RH)	0/59 post 100 hrs
	L3 Precon + add'l Pb-free reflows	0/39 post 10x add'l reflows
22x22 mm	L3 Precon + TCB (-55°C / +125°C)	0/95 post 700 cycles
	L3 Precon + HAST (130°C/85% RH)	0/56 post 100 hrs
	L3 Precon + add'l Pb-free reflows	0/21 post 10x add'l reflows

Table 4: Enabled BGA package reliability results for nHF vs. HF packages

Substrate Form Factor	Reliability Stress	HF Fails	nHF Fails
13x14 mm	Shock Test (40 mil test board, 5 drops, 295G input)	0/9 CTF cracking	0/9 CTF cracking
	Temp Cycle test (-25 to +100°C)	0/8 through 2500 cycles	0/8 through 2500 cycles

Table 5: Core material UL-94 flammability rating after extended Pb-free reflows

Core Mat'l	Criteria	Number of Reflows at 260°C		
		0	5x	10x
Halogenated	Passed V-0 criteria?	Yes	Yes	Yes
HF		Yes	Yes	Yes

Electrical Performance

Lastly, from a performance standpoint, nHF and HF components were tested side by side to determine the electrical impact of an HF core. Test results confirmed no impact on maximum operating frequency due to the use of an HF core, and electrical performance parity between nHF and HF was achieved.

In summary, a careful choice of HF core materials enabled Intel to introduce and ramp HF-compliant substrates that met assembly processing requirements as well as use condition component and board-level reliability requirements while maintaining the electrical performance of the package. Additionally, the selection of HF core materials with similar properties to nHF core materials enabled Intel to use existing recipes for component and board-mount assembly. This reduces the impact on the factory, and it potentially minimizes the impact on board-mount processes at customer sites due to the use of HF substrates.

CONCLUSION

The implementation of Pb-free and HF-compliant packaging materials is critical to Intel, and it is vital to Intel's broader strategy to support an environmentally sustainable future for its industry. Enabling of Pb-free materials with robust resistance to Pb-free assembly processing was made possible through prudent downselection of solder TIM materials, FLI solder, and substrate materials, 2LI ball attach and surface-mount paste materials, and BGA solder metallurgy. The transition to HF-compliant substrate materials posed significant assembly and reliability challenges that were addressed and successfully met. The transition to Pb-free packaging and HF-compliant substrate materials was achieved through close collaboration with industry partners, suppliers, and our customer base, and we had to establish a robust materials supply infrastructure to sustain the environmentally green micro-electronic packaging ecosystem. The adoption of these initiatives has maintained Intel's OGA philosophy in micro-electronic packaging.

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